Title: MEMORY CIRCUIT WITH REDUNDANT CONFIGURATION
Inventor: TSUKIDATE, et al.
Application No. Unknown
Docket No. 108066-00100

FIG. 1A

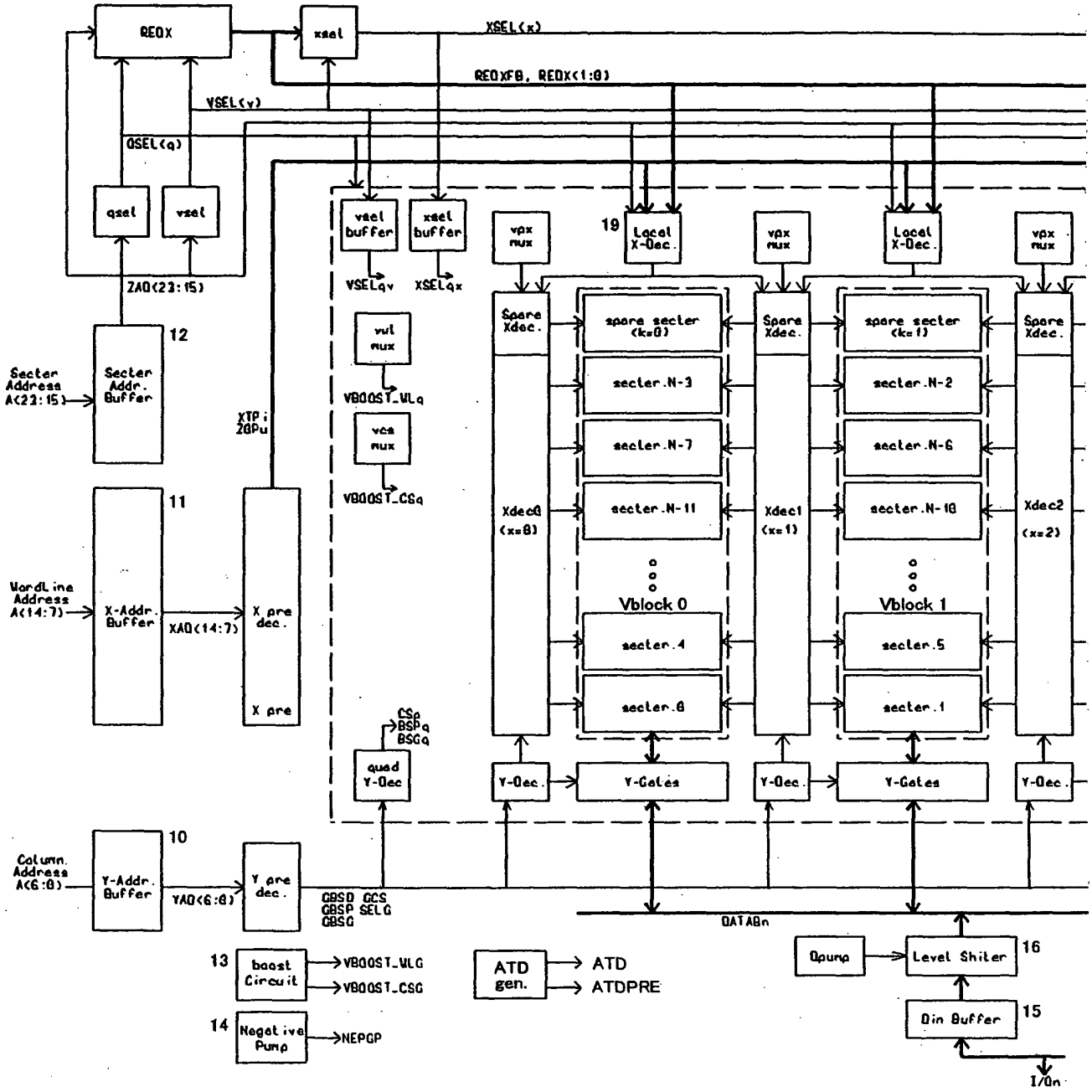


FIG. 1B

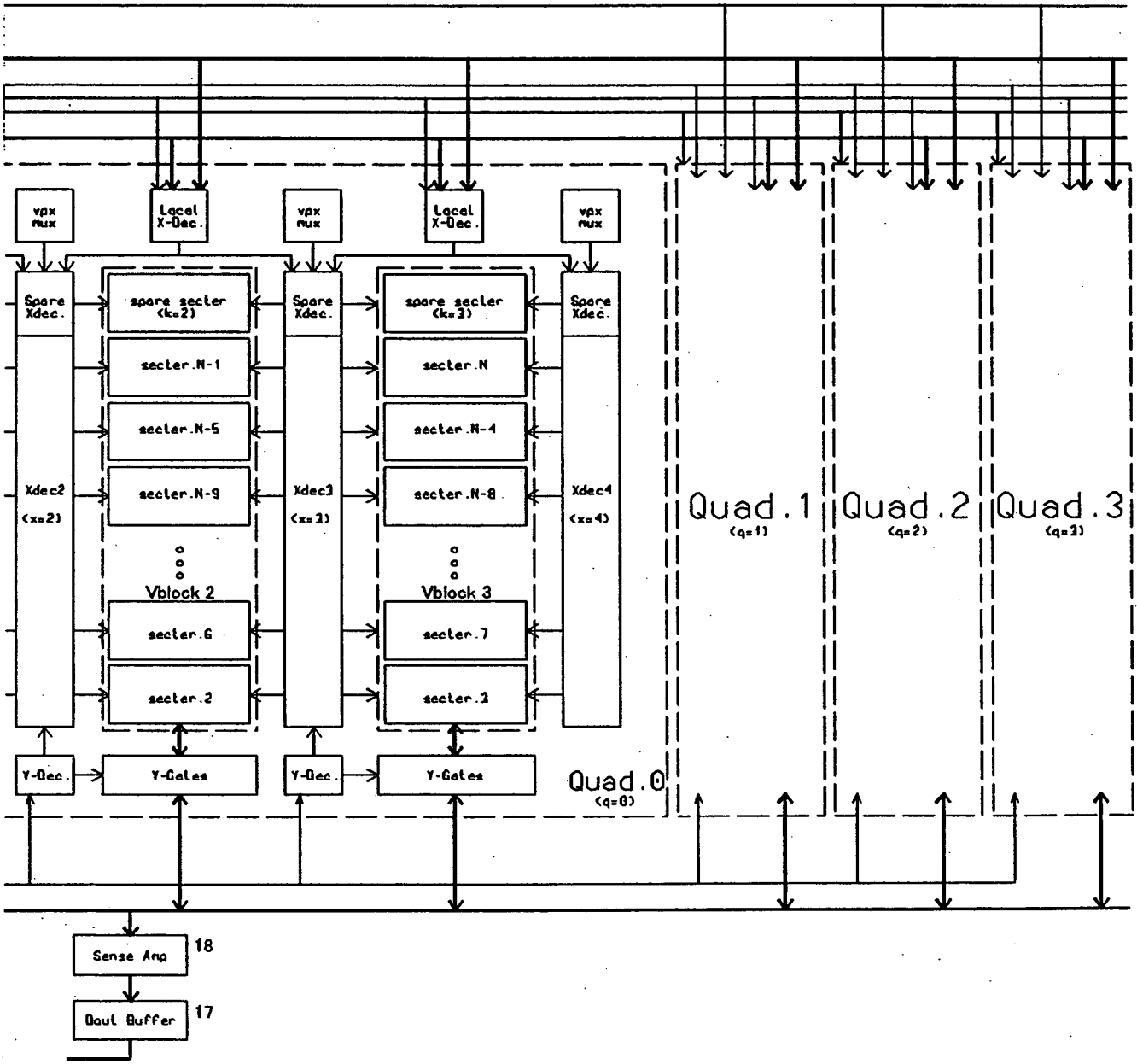

vgx mux
Local X-Dec.
vgx mux
Local X-Dec.
vgx mux
Spare Xdec.
spare secter (k=2)
secter.N-1
secter.N-5
secter.N-9
Xdec2 (x=2)
Vblock 2
secter.6
secter.2
Spare Xdec.
Xdec3 (x=3)
Spare Xdec.
spare secter (k=3)
secter.N
secter.N-4
secter.N-8
Vblock 3
secter.7
secter.3
Xdec4 (x=4)
Quad.1 (q=1)
Quad.2 (q=2)
Quad.3 (q=3)
Y-Dec.
Y-Gates
Y-Dec.
Y-Gates
Quad.0 (q=0)
Sense Amp
18
Dout Buffer
17

FIG. 2A

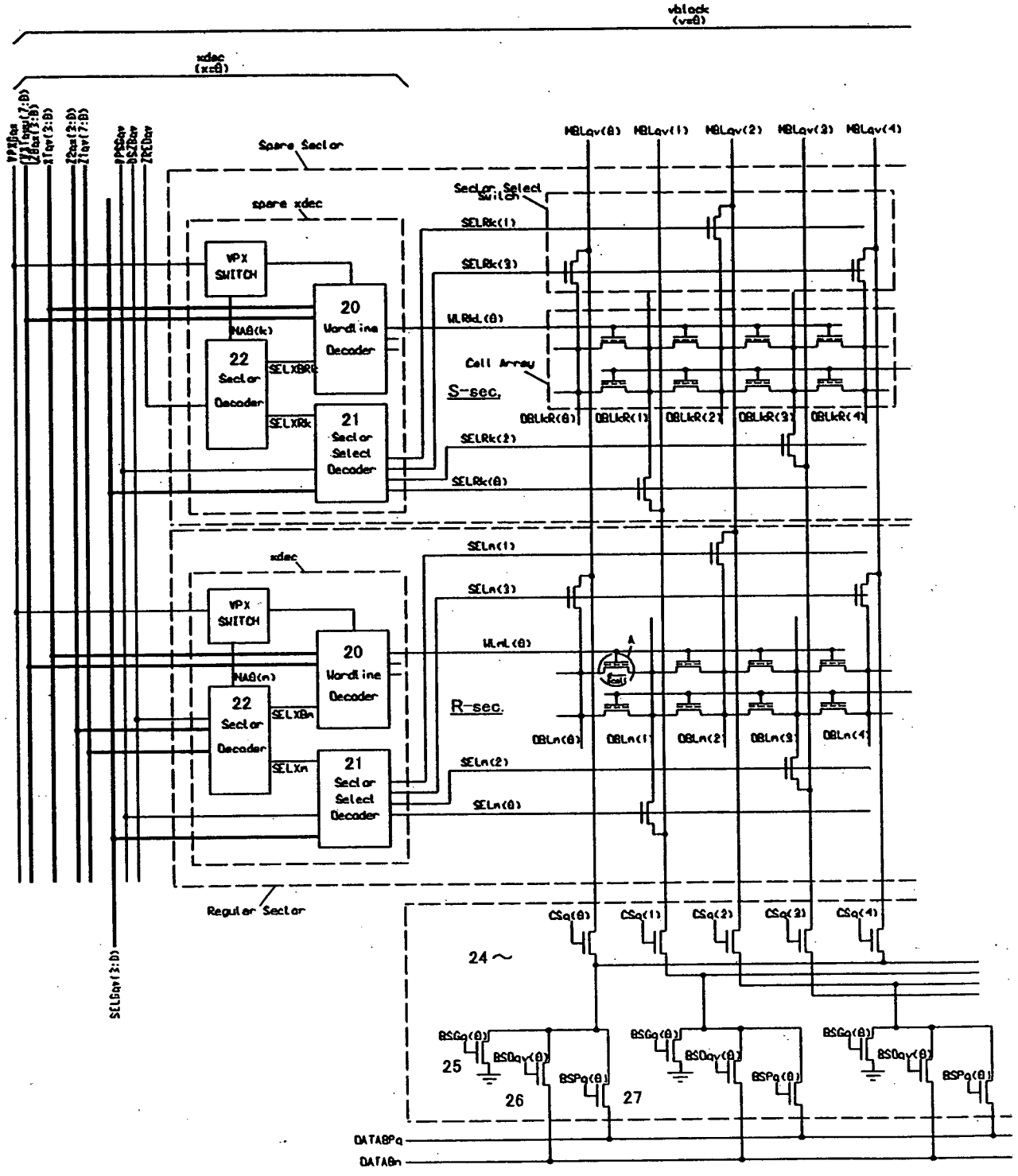

vblock (v=0)
xdec (x=0)
Spare Sector
spare xdec
VPX SWITCH
20 Wordline Decoder
22 Sector Decoder
21 Sector Select Decoder
Sector Select Switch
SELRk(1)
SELRk(3)
WLRkL(0)
Cell Array
S-sec.
SELXBRk
SELXRk
SELRk(2)
SELRk(0)
MBLqv(0)
MBLqv(1)
MBLqv(2)
MBLqv(3)
MBLqv(4)
DBLkR(0)
DBLkR(1)
DBLkR(2)
DBLkR(3)
DBLkR(4)
xdec
SELn(1)
SELn(3)
WLnL(0)
R-sec.
SELXBn
SELXn
SELn(2)
SELn(0)
DBLn(0)
DBLn(1)
DBLn(2)
DBLn(3)
DBLn(4)
Regular Sector
CSq(0)
CSq(1)
CSq(2)
CSq(3)
CSq(4)
24
BSGq(0)
BSDqv(0)
BSPq(0)
25
26
27
DATABPq
DATABn
SELBqv[2:0]

FIG. 2B

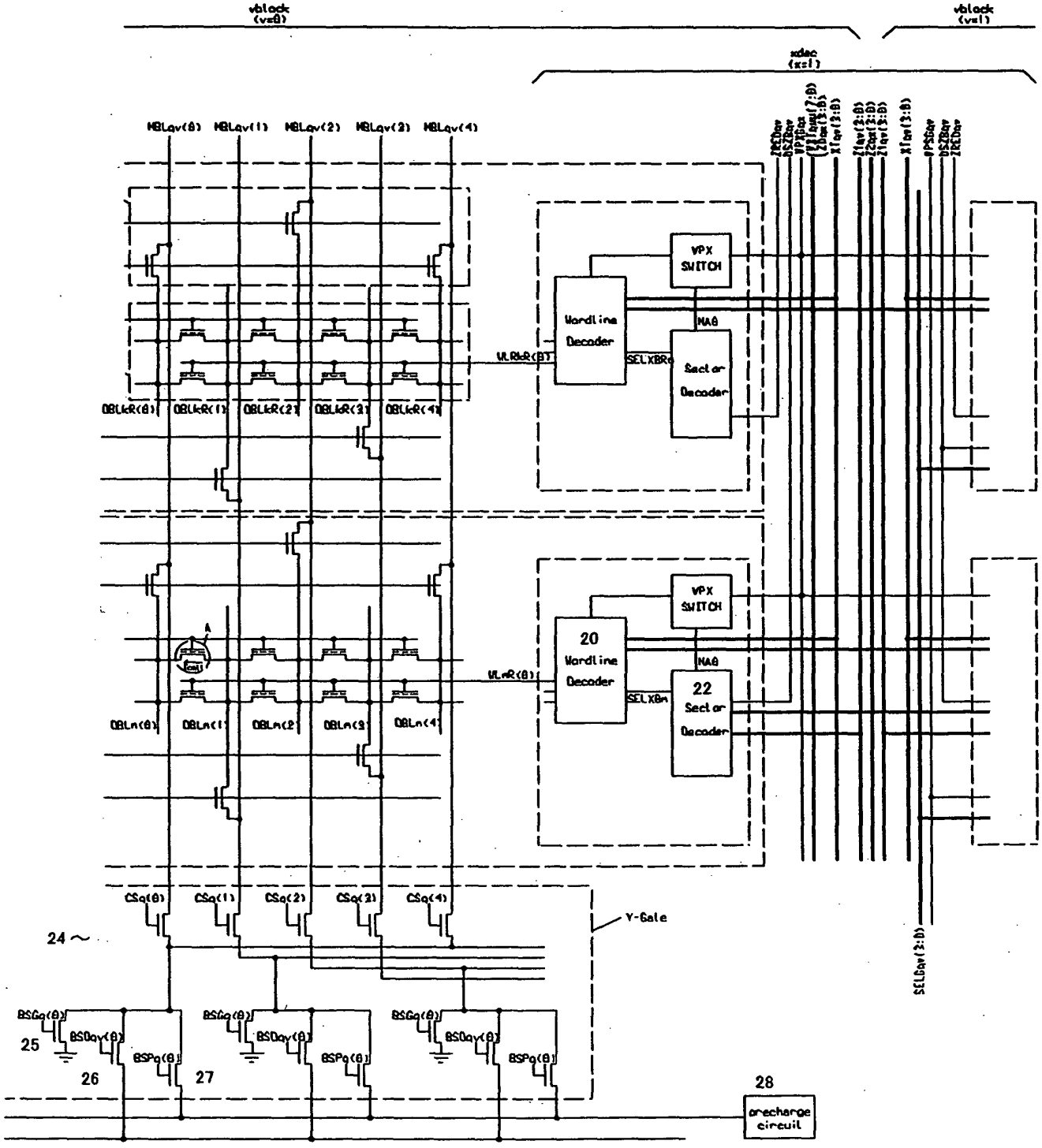

vblock (v=0)
vblock (v=1)
xdec (x=1)
MBLav(0)
MBLav(1)
MBLav(2)
MBLav(3)
MBLav(4)
VPX SWITCH
Wordline Decoder
NA0
Sector Decoder
VLRLR(0)
SELXBR0
OBLLR(0)
OBLLR(1)
OBLLR(2)
OBLLR(3)
OBLLR(4)
20
22
VLWR(0)
SELXBn
OBLn(0)
OBLn(1)
OBLn(2)
OBLn(3)
OBLn(4)
CSa(0)
CSa(1)
CSa(2)
CSa(3)
CSa(4)
Y-Gate
24
BSGa(0)
BSOav(0)
BSPa(0)
25
26
27
28
precharge circuit
SELBav(3:0)

FIG. 3

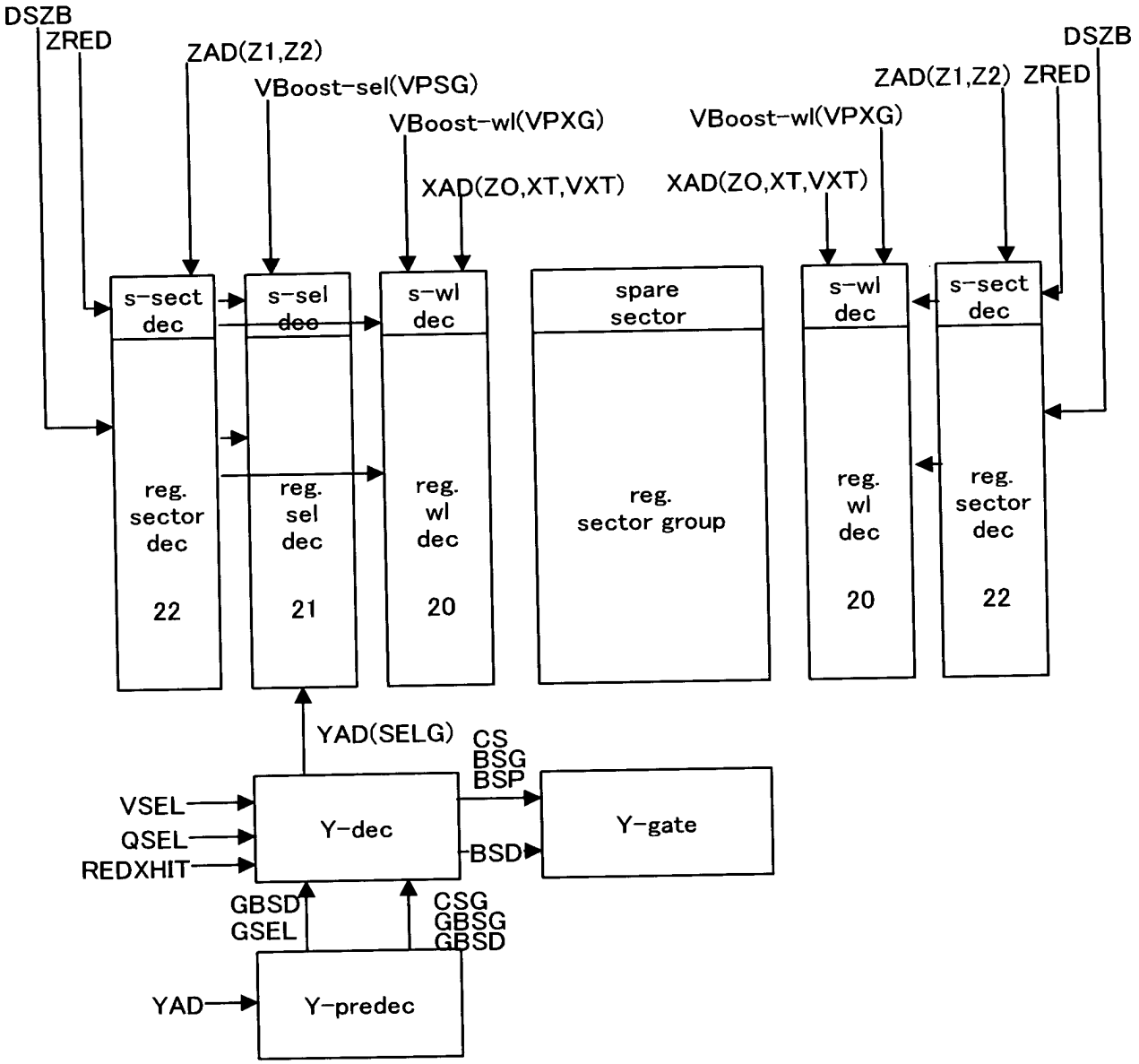

DSZB
ZRED
ZAD(Z1,Z2)
VBoost-sel(VPSG)
VBoost-wl(VPXG)
XAD(ZO,XT,VXT)
VBoost-wl(VPXG)
XAD(ZO,XT,VXT)
ZAD(Z1,Z2)
ZRED
DSZB
s-sect dec
s-sel dec
s-wl dec
spare sector
s-wl dec
s-sect dec
reg. sector dec
22
reg. sel dec
21
reg. wl dec
20
reg. sector group
reg. wl dec
20
reg. sector dec
22
YAD(SELG)
CS
BSG
BSP
VSEL
QSEL
REDXHIT
Y-dec
BSD
Y-gate
GBSD
GSEL
CSG
GBSG
GBSD
YAD
Y-predec

FIG. 4

Simultaneously Selected State for Regi WL and Spare WL

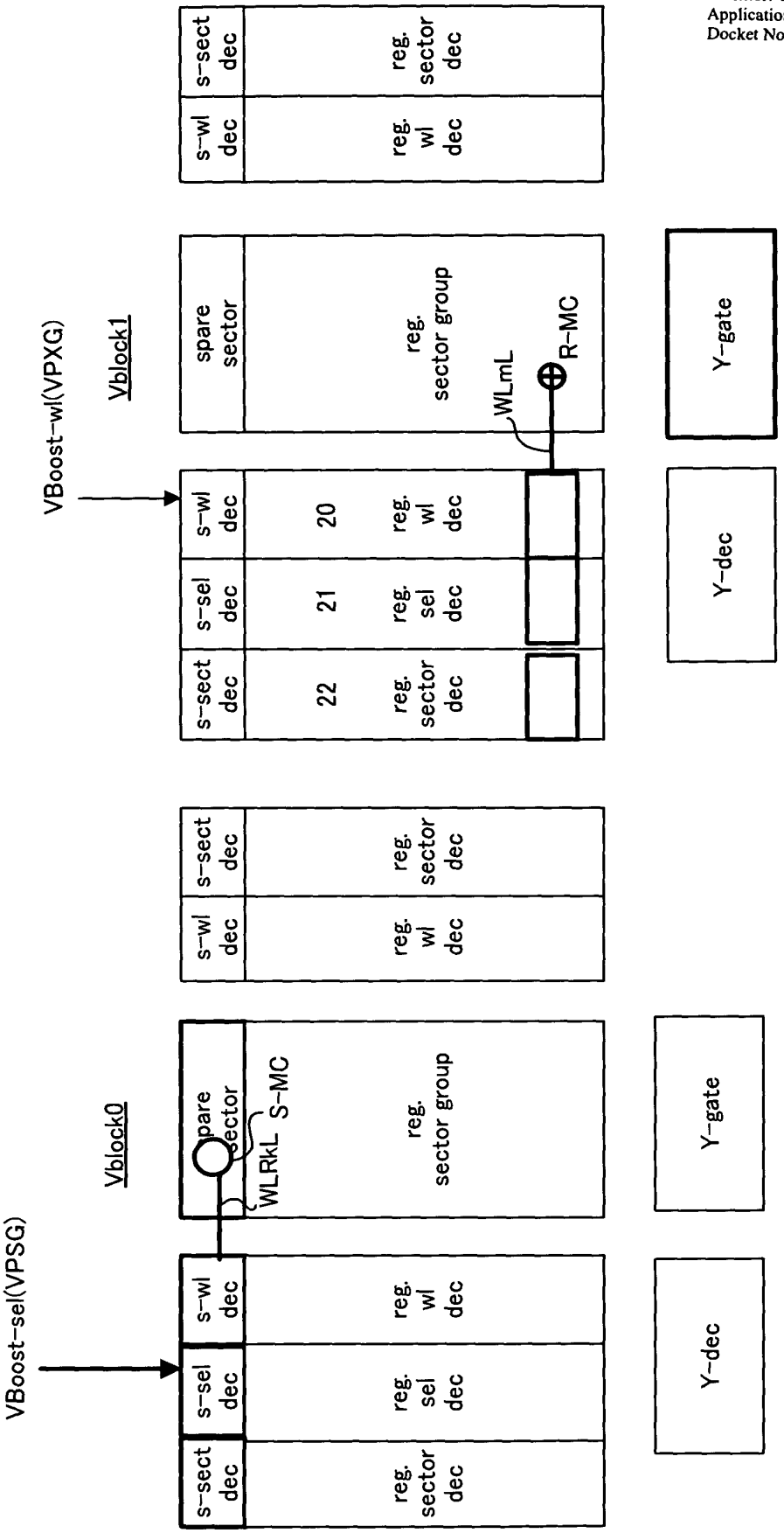
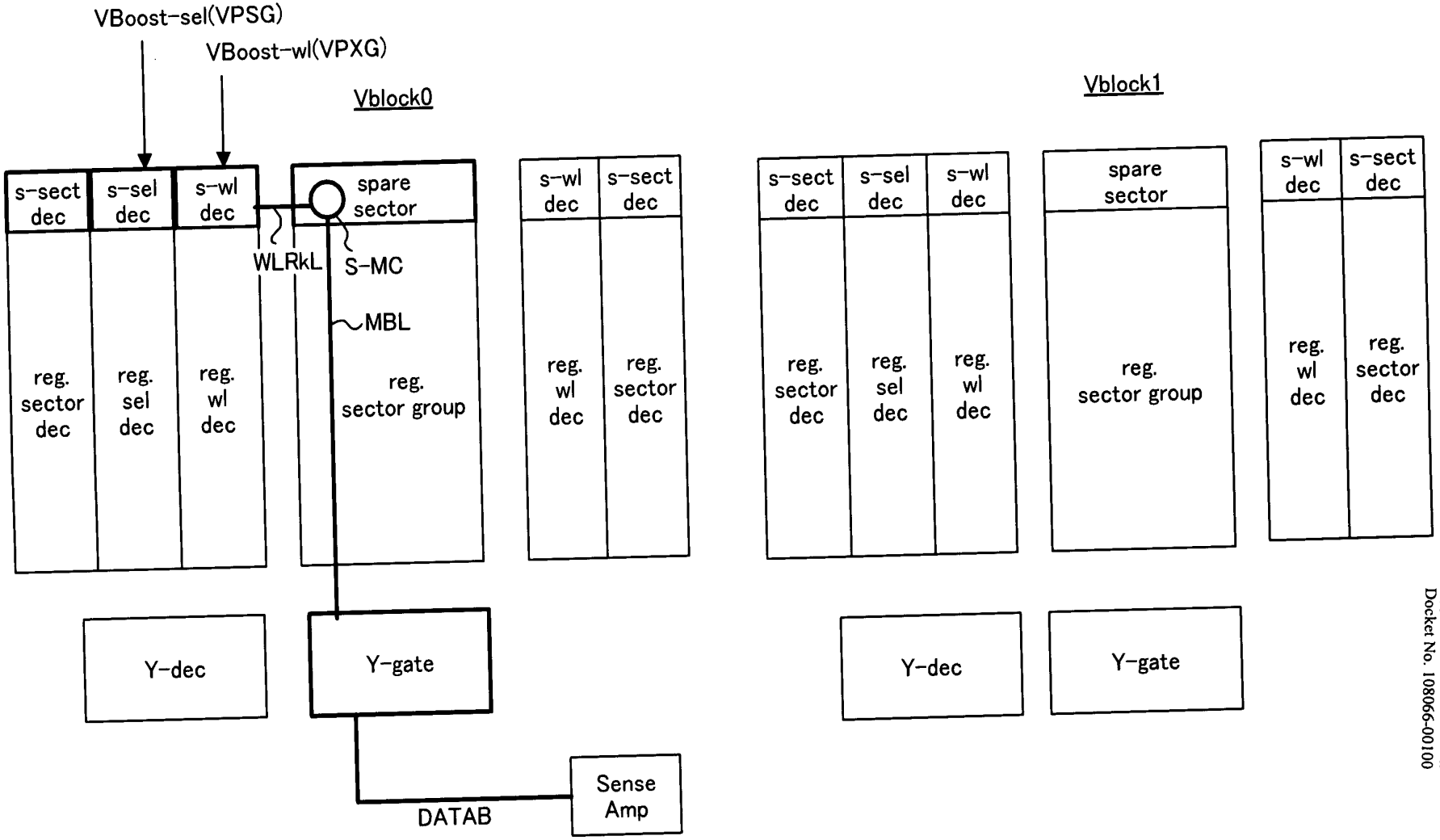


FIG. 5

Redundancy Address is Matched



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Application No. Unknown
Docket No. 108066-00100

FIG. 6

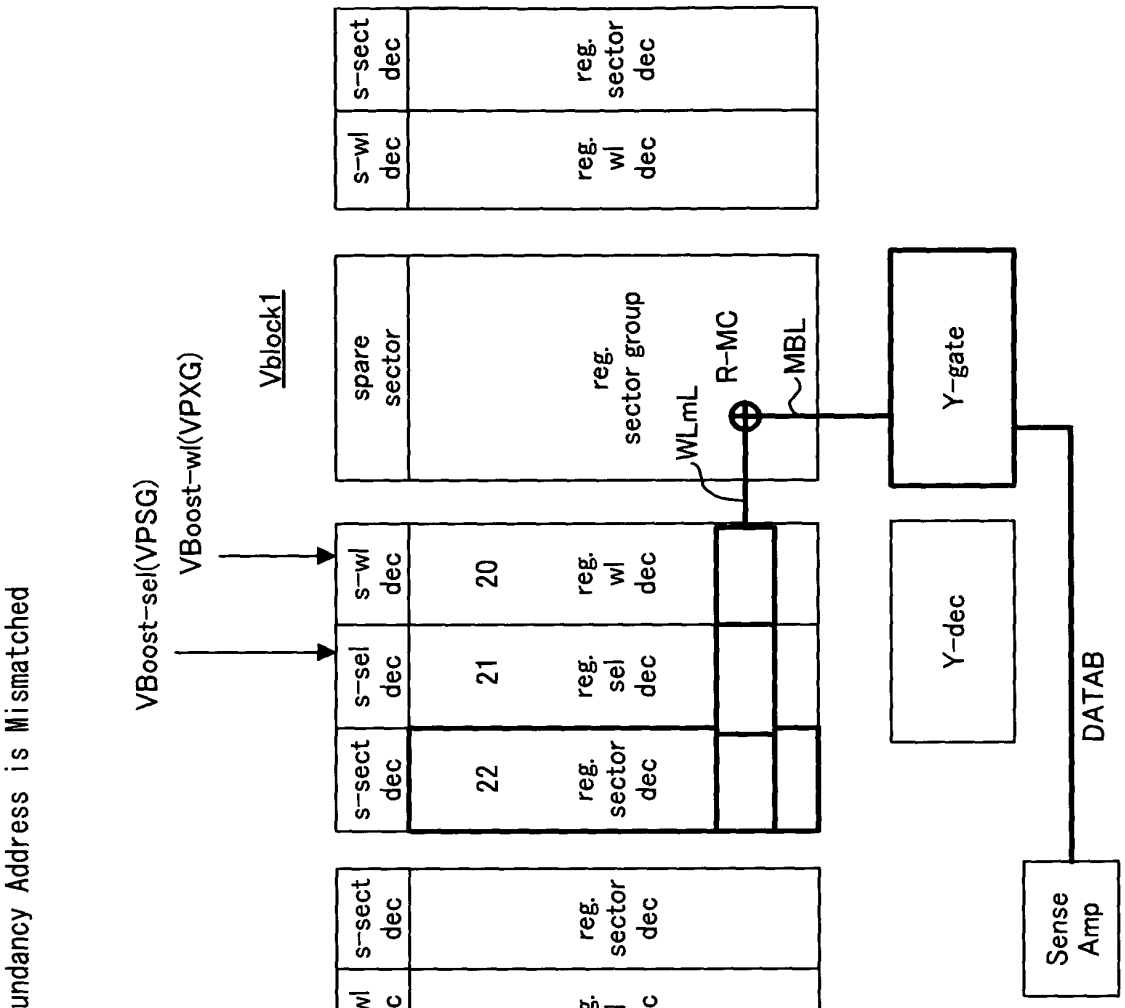

Redundancy Address is Mismatched
VBoost-sel(VPSG)
VBoost-wl(VPXG)
Vblock1
Vblock0
s-sect dec
s-sel dec
s-wl dec
reg. sector dec
reg. sel dec
reg. wl dec
spare sector
reg. sector group
22
21
20
WLmL
R-MC
MBL
Y-gate
Y-dec
DATAB
Sense Amp

FIG. 7 Vertical Block Select Signal Buffer Circuit

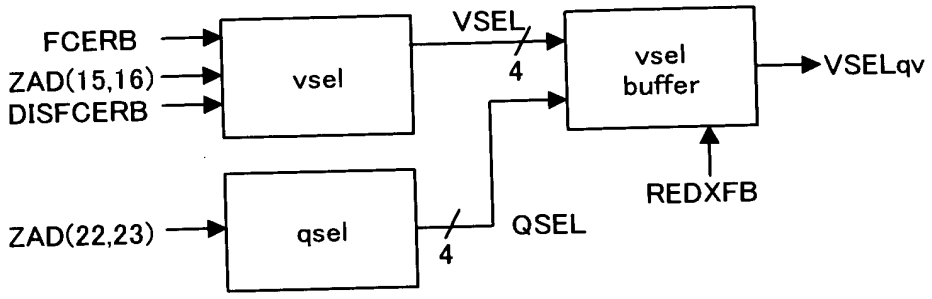
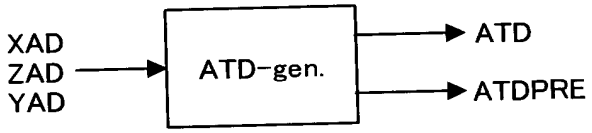


FIG. 8



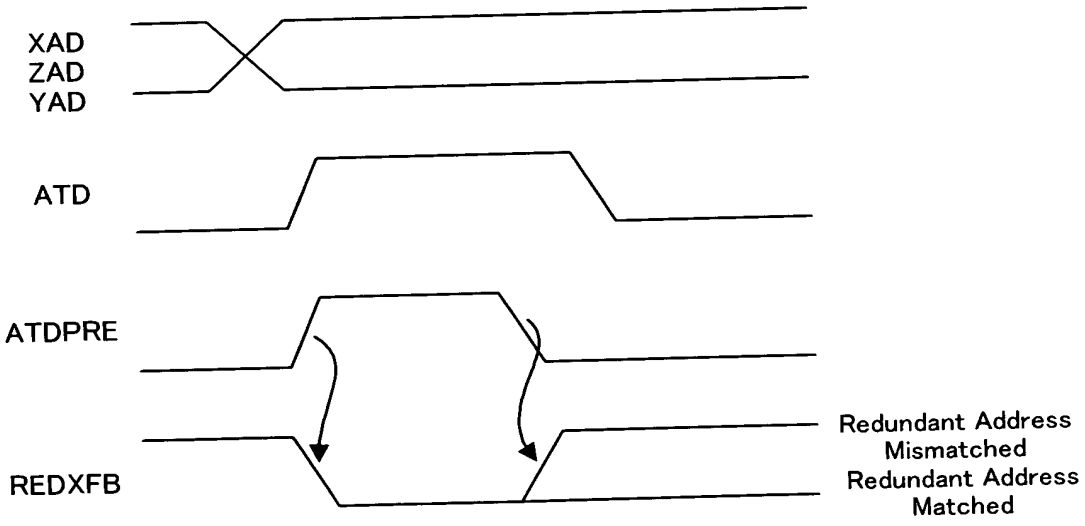


FIG. 9

Redundancy Judgment Circuit

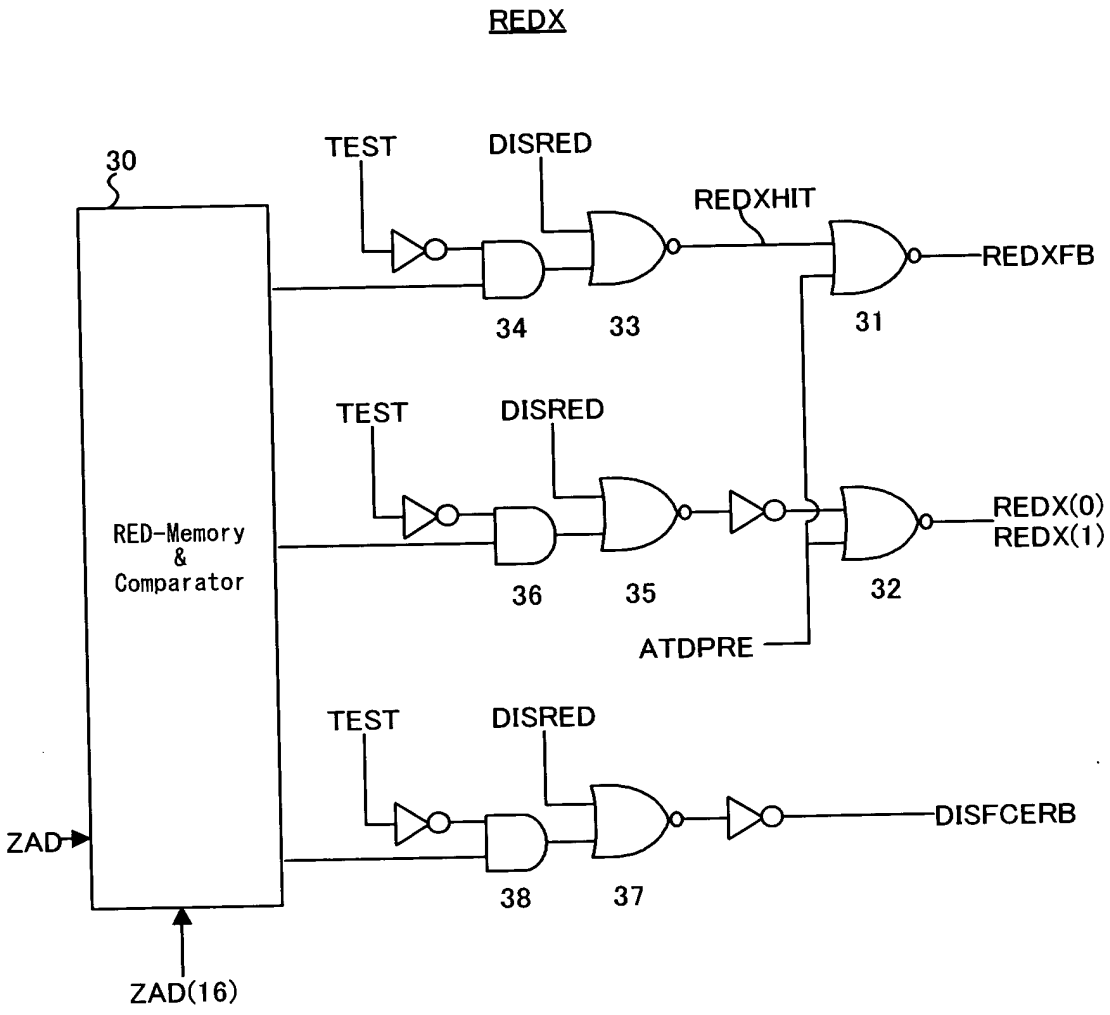


FIG. 10

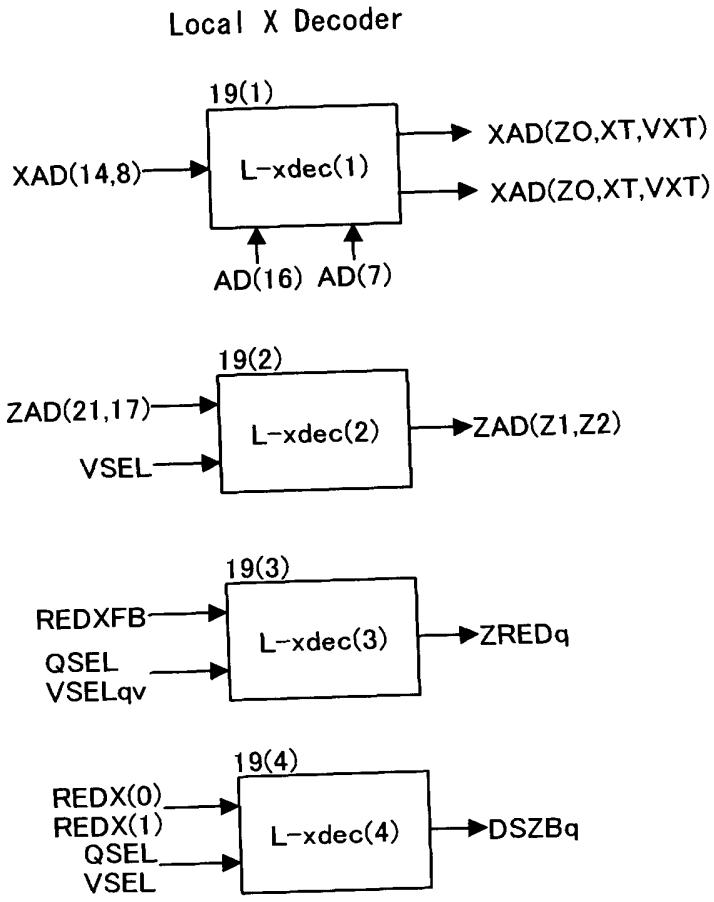

Local X Decoder
19(1)
XAD(14,8)
L-xdec(1)
XAD(ZO,XT,VXT)
XAD(ZO,XT,VXT)
AD(16)
AD(7)
19(2)
ZAD(21,17)
VSEL
L-xdec(2)
ZAD(Z1,Z2)
19(3)
REDXFB
QSEL
VSELqv
L-xdec(3)
ZREDq
19(4)
REDX(0)
REDX(1)
QSEL
VSEL
L-xdec(4)
DSZBq

FIG. 11

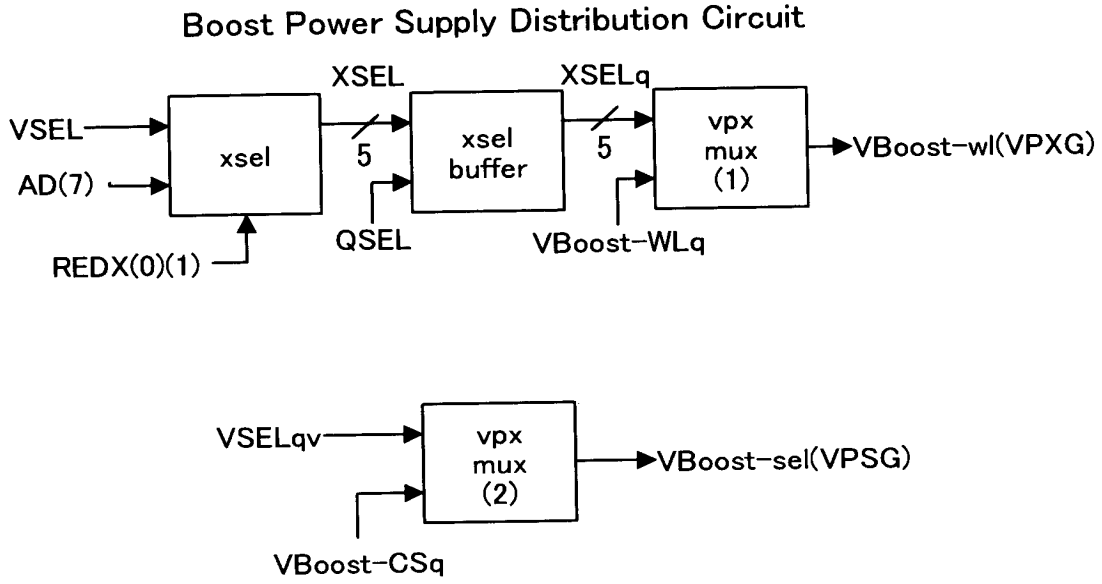

Boost Power Supply Distribution Circuit
XSEL
XSELq
VSEL
xsel
5
xsel buffer
5
vpx mux (1)
VBoost-wl(VPXG)
AD(7)
QSEL
VBoost-WLq
REDX(0)(1)
VSELqv
vpx mux (2)
VBoost-sel(VPSG)
VBoost-CSq

FIG. 12

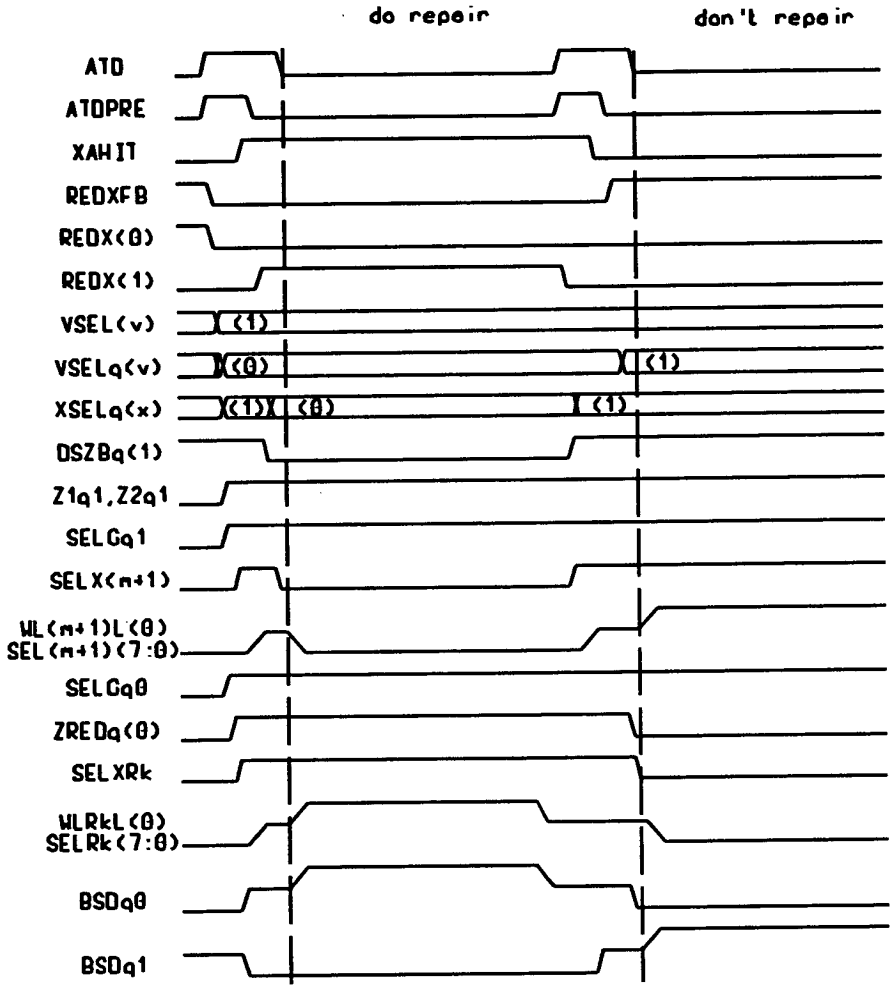

do repair
don't repair
ATD
ATDPRE
XAHIT
REDXFB
REDX(0)
REDX(1)
VSEL(v)
VSELq(v)
XSELq(x)
DSZBq(1)
Z1q1,Z2q1
SELGq1
SELX(m+1)
WL(m+1)L(0)
SEL(m+1)(7:0)
SELGq0
ZREDq(0)
SELXRk
WLRkL(0)
SELRk(7:0)
BSDq0
BSDq1

FIG. 13A

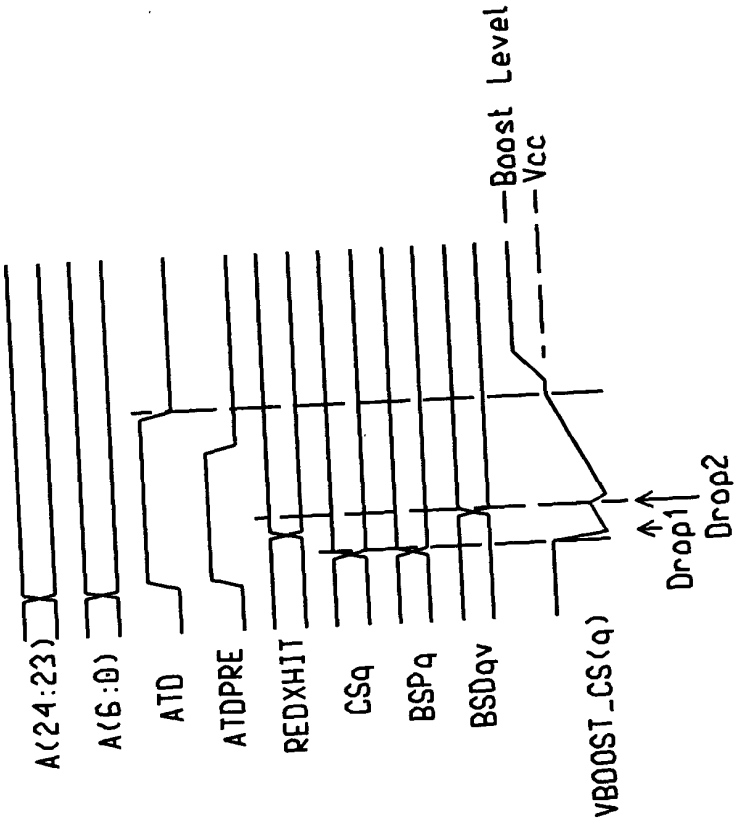


FIG. 13B

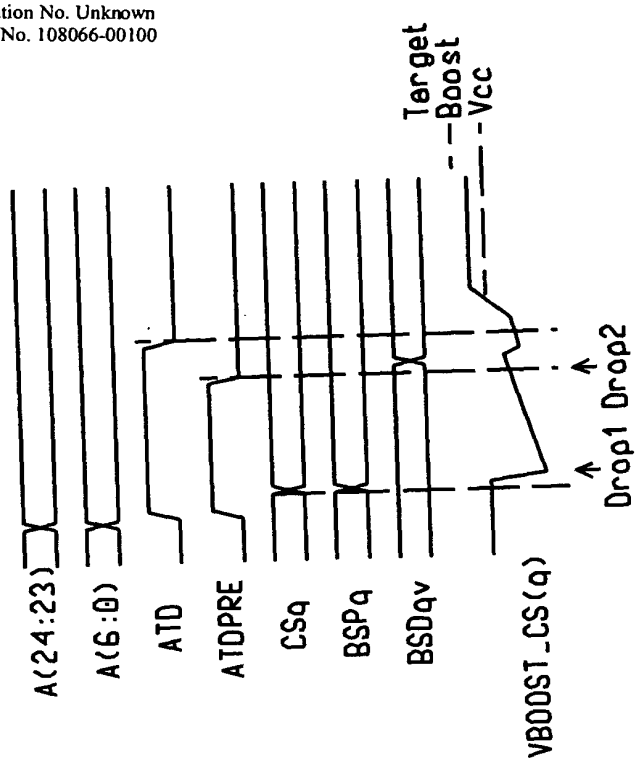
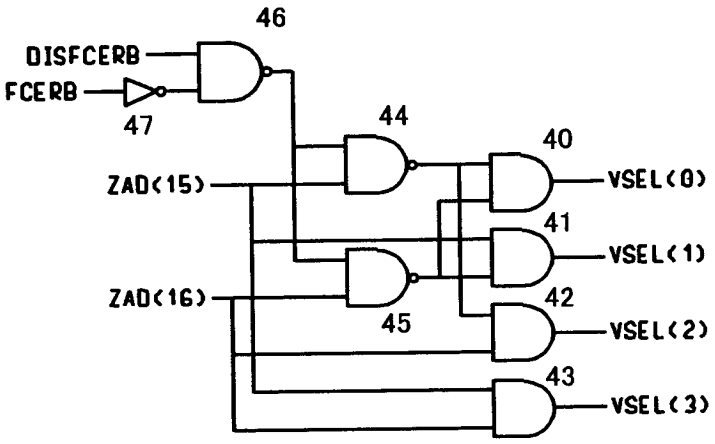


FIG. 14


vsel
46
DISFCERB
FCERB
47
44
40
ZAD(15)
VSEL(0)
41
VSEL(1)
ZAD(16)
45
42
VSEL(2)
43
VSEL(3)